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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/197,534	11/23/1998	SHUNPEI YAMAZAKI	0756-1894	1382

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/197,534	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2002* .

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/709,108* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☒ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *16, 21* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidemi et al., Japanese Patent Abstracts 03-159119.

4. Pertaining to claim 1, Hidemi discloses a semiconductor process as claimed. See **FIGS. 1(a)-1(c)**, where Hidemi teaches a method of manufacturing a semiconductor device comprising the steps of:

preparing a plurality of semiconductor islands over a glass substrate **1**;

subjecting said semiconductor islands to an ion doping;

directing a pulsed laser beam having a cross section elongated in one direction to said glass substrate;

moving said glass substrate in a direction perpendicular to the elongation direction of said pulsed laser beam, thereby irradiating said semiconductor islands with said pulsed laser beam.

5. Pertaining to claim 2, Hidemi teaches wherein an energy density of said pulsed laser beam is not higher than 300 mJ/cm^2 (please note in section 5, Hidemi teaches a XeCl pulsed laser beam with an energy density of 250 mJ/cm^2).

6. Pertaining to claim 3, Hidemi teaches wherein an impurity selected from the group consisting of phosphorous and boron is selectively introduced into said plurality of semiconductor islands by said ion doping.

7. Pertaining to claim 4, Hidemi teaches wherein each of said semiconductor islands is irradiated with plural pulses of said pulsed layer beam.

8. Pertaining to claim 5, Hidemi teaches a method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film **12** over a glass substrate **1**;

crystallizing said semiconductor film;

patterning the crystallized semiconductor film into a plurality of semiconductor islands;

subjecting said semiconductor islands to an ion doping;

directing a pulsed laser beam having a cross section elongated in one direction to said glass substrate (i.e., performing a shallow doping of only the source/drain region);

moving said glass substrate in a direction perpendicular to the elongation direction of said pulsed laser beam, thereby irradiating said semiconductor islands with said pulsed laser beam

9. Pertaining to claim 6, Hidemi teaches wherein an energy density of said pulsed laser beam is not higher than 300 mJ/cm^2.

10. Pertaining to claim 7, Hidemi teaches wherein an impurity selected from the group consisting of phosphorus and boron is selectively introduced into said plurality of semiconductor islands.

11. Pertaining to claim 8, Hidemi teaches wherein each of said semiconductor islands is irradiated with plural pulses of said pulsed laser beam.

12. Pertaining to claim 13, Hidemi teaches a method of manufacturing a semiconductor device comprising the steps of:

preparing a plurality of semiconductor islands over a glass substrate **1**;

forming a film comprising silicon oxide 13 over said glass substrate wherein said semiconductor island are covered by said film;

subjecting said semiconductor islands to an ion doping through said film;

directing a pulsed laser beam having a cross section elongated in one direction to said glass substrate;

moving said glass substrate in a direction perpendicular to the elongation direction of said pulsed laser beam, thereby irradiating said semiconductor islands with said pulsed laser beam through said film.

13. Pertaining to claim 14, Hidemi teaches wherein an energy density of said pulsed laser beam is not higher than 300 mJ/cm^2.

14. Pertaining to claim 15, Hidemi teaches wherein an impurity selected from the group consisting of phosphorus and boron is selectively introduced into said plurality of semiconductor islands by said ion doping.

15. Pertaining to claim 16, Hidemi teaches wherein each of said semiconductor islands is irradiated with plural pulses of said pulsed laser beam.

16. Pertaining to claims 21 and 22, Hidemi teaches wherein said pulsed laser beam is a pulsed excimer laser beam (it is well known that a xenon-chloride laser is a pulsed excimer laser beam).

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidemi Japanese Abstract Publication 03-159119 in view of Nakazawa U.S. Patent 5,561,075.

19. Pertaining to claims 9-12 and 24, Hidemi discloses a semiconductor process substantially as claimed. Hidemi teaches a method of manufacturing a semiconductor device comprising the steps of:

preparing a plurality of first semiconductor islands over a glass substrate;

subjecting the semiconductor island to a first ion doping for introducing a first impurity;

directing a pulsed laser beam having a cross section elongated in one direction to said glass substrate;

moving said glass substrate in a direction perpendicular to the elongation direction of said pulsed laser beam, thereby irradiating semiconductor islands with said pulsed laser beam. However, Hidemi fails to teach forming a plurality of second semiconductor islands and subjecting the second semiconductor islands to a doping that is opposite in conductivity type to

said first impurity. Nakazawa teaches forming a first type and second type of semiconductor islands having conductivity different from each other. See column 3, lines 35-40 where Nakazawa teaches the fabrication of first (n-type, i.e., phosphorus) and second islands (p-type, i.e., boron) of a semiconductor device. In view of Nakazawa, it would have been obvious to one of ordinary skill in the art to incorporate first type islands and second type islands into the Hidemi semiconductor process because the claimed process will produce a CMOS inverter and memory cell circuits (column 3, lines 35-40).

20. Pertaining to claim 10, Hidemi teaches wherein an energy density of said pulsed laser beam is not higher than 300 mJ/cm^2.

21. Pertaining to claim 12, Hidemi teaches wherein each of said semiconductor islands is irradiated with plural pulses of said pulsed laser beam.

22. Pertaining to claim 24, Hidemi teaches wherein said pulsed laser beam is a pulsed excimer laser beam.

23. Claims 17, 18, 19, 20, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hidemi et al., Japanese Patent Abstracts 03-159119 in view of Czubatyj et al., U.S. Patent 5,180,690.

24. Pertaining to claims 17 and 19, Hidemi discloses a semiconductor process substantially as claimed. Hidemi teaches a method of manufacturing a semiconductor device comprising the steps of:

preparing a plurality of semiconductor islands over a glass substrate 1;

forming a film comprising silicon oxide 13 over said glass substrate wherein said semiconductor island are covered by said film;

subjecting said semiconductor islands to an ion doping through said film;

directing a pulsed laser beam having a cross section elongated in one direction to said glass substrate;

moving said glass substrate in a direction perpendicular to the elongation direction of said pulsed laser beam, thereby irradiating said semiconductor islands with said pulsed laser beam through said film. However, Hidemi fails to teach semiconductor island comprising silicon and germanium over a substrate. Czubatyj teaches forming a semiconductor island comprising silicon and germanium over a substrate. See column 3, lines 49-55 of Czubatyj where an alloy of silicon and germanium are made for the fabrication of a semiconductor device. In view of Czubatyj it would have been obvious to one of ordinary skill in the art to incorporate silicon and germanium into the Hidemi semiconductor process because a body of semiconductor alloy material can be deposited on a low temperature glass substrate (column 3, lines 49-65).

25. Pertaining to claim 18, Hidemi teaches wherein an impurity selected from the group consisting of phosphorus and boron is selectively introduced into said plurality of semiconductor islands by said ion doping.

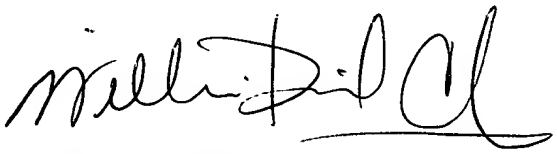
26. Pertaining to claims 20, 25 and 26, Hidemi teaches wherein said pulsed laser beam is a pulsed excimer laser beam (it is well known that a xenon-chloride laser is a pulsed excimer laser beam).

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.



W. David Coleman
Examiner
Art Unit 2823

WDC
July 1, 2002